Self-Timed Reconfigurable Hardware

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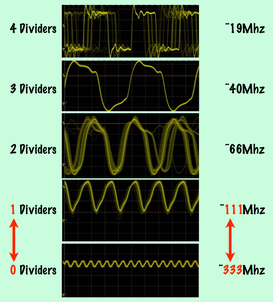
1. The simplest possible self-timed circuit is a ring oscillator.

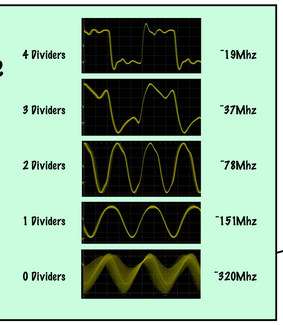
Although this circuit oscillates, the resulting signal frequency is too high to sample at the I/O pads, or even to easily divide down to lower frequencies.



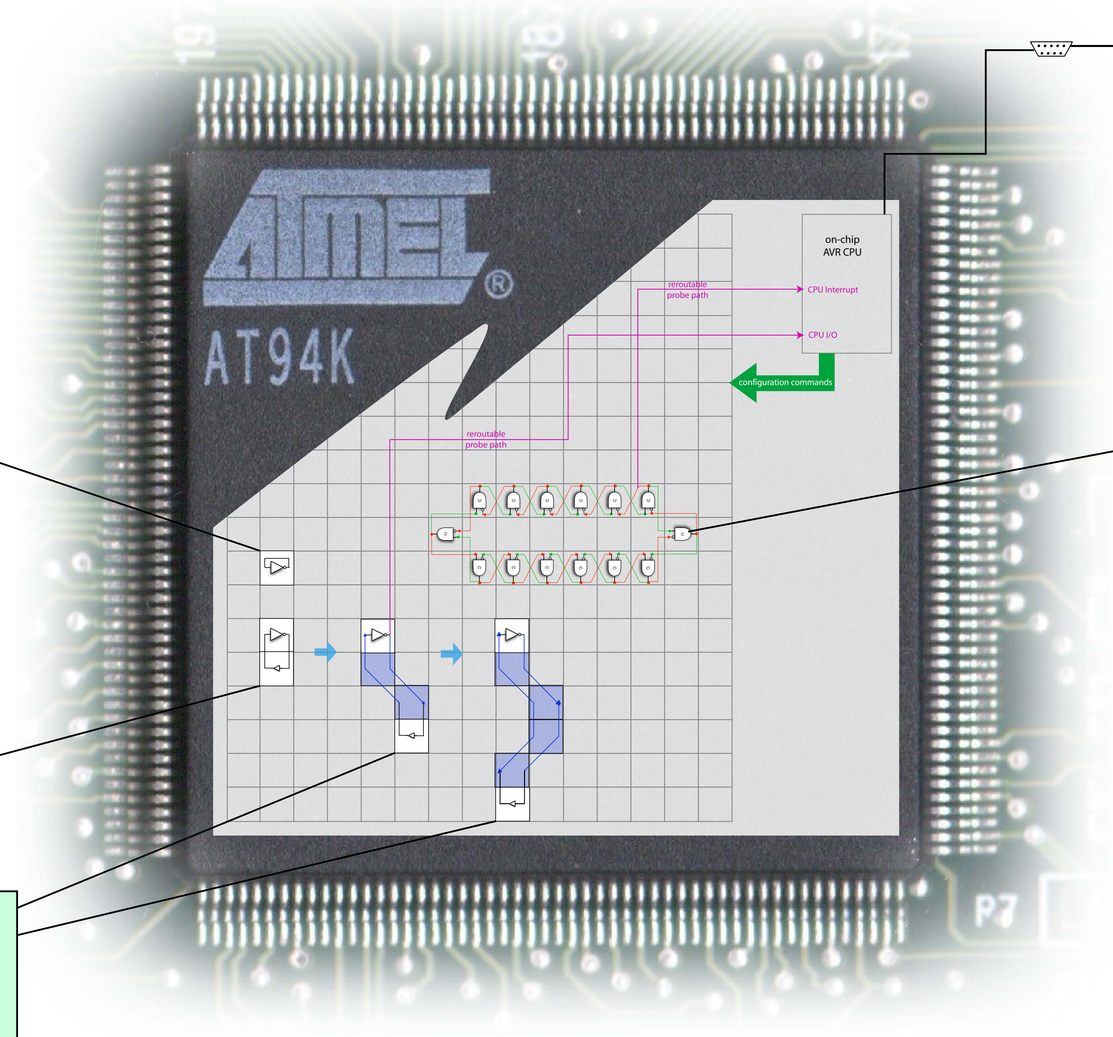
Frequency Division Fails

2. By including a one-cell buffer loop, we can reduce the oscillation to a manageable frequency.

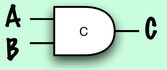
Inserting frequency dividers yields a signal that can be cleanly sampled at the I/O pad.



3. Additional delay loops and repeated measurements are used to confirm the accuracy of previous measurements



4. A Muller C Element is a stateful gate. When both its inputs are the same, its output takes on that value. When its outputs differ, it retains its previous value.

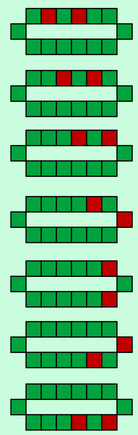


A	B	C
0	0	0
0	1	C
1	0	C
1	1	1

5. With one input inverted, Muller C Elements can be linked in a ring.

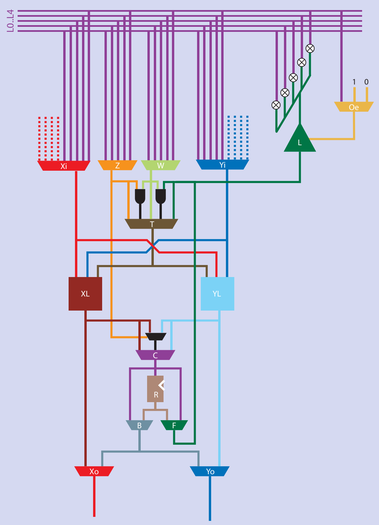
Just like an inverter ring, wavefronts will propagate around the C-element ring at the maximum rate allowed by the circuitry.

Unlike an inverter ring, the C-element protocol preserves boundaries between distinct wavefronts -- they extert "backpressure" and will not collide.



Atmel's FPGAs are the only commercial devices with a public bitstream format. This is essential for implementing exotic circuits and dynamic, on-line tools.

This device also includes two other unique features: fine-grained partial reconfiguration and a cell-local combinational feedback line



6. This graph shows the number of wavefronts passing a fixed point on the ring (per second) as a function of the percent occupancy of the ring (how many wavefronts it holds)

The green and red wires shown in the diagram are routed along different channels, each having a different delay. This asymmetry can be observed in the graph; reversing the assignment of inputs-to-wires causes the graph to reverse.

The velocity of wavefronts in the ring is greatest when the ring occupancy is lowest (one wavefront). At this occupancy, the wavefront moves around the ring at a rate of 540Mcells/sec on Atmel's 350nm FPGA.